SPECIFICATIONS
FOR
EPD MODULE

CUSTOMER	
MODEL	**SCP075001-V01**
CUSTOMER APPROVED	

APPROVED BY	CHECKED BY	ORGANIZED BY
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Revision History

Revision	Description	Date
A0	First Version Release	2021.10.22

Glossary of Acronyms

EPD	Electrophoretic Display (e-Paper Display)
EPD Panel	EPD
T-Con	Timing Contrer
TFT	Thin Film Transistor
MCU	Microcontroller Unit
FPC	Flexible Printed Circuit
FPL	Front Plane Laminate
SPI	Serial Peripheral Interface
COG	Chip on Glass

1.General Description

1.1 Overview

This is a 3-Colors 7.5” a-Si, active matrix TFT, Electronic Paper Display (EPD) panel. The panel has such high resolution (124dpi) that it is able to easily display fine patterns. Due to its bi-stable nature, the EPD panel requires very little power to update and needs no power to maintain an image.

1.2 Feature

1.2.1 a-Si TFT active matrix Electronic Paper Display(EPD)

1.2.2 Three colors support: White, Black, Red

1.2.3 Resolution:800 x 480

1.2.4 Ultra-low power consumption

1.2.5 Super Wide Viewing Angle - near 180°

1.2.6 Extra thin & light

1.2.7 SPI interface

1.2.8 RoHS compliant

1.3 General Specifications

Item	Specification	Unit	Note
Outline Dimension	170.2(H) x 111.2(V) x 1.1(T)	mm	(1)
Active Area	163.2(H) x97.92(V)	mm	
Driver Element	a-Si TFT active matrix	-	
FPL	Spectra Red R2.0	-	
Pixel Number	800 x 480	pixel	
Pixel Pitch	204x 204 (124dpi)	um	
Pixel Arrangement	Vertical stripe	-	
Display Colors	Black/White/Red	-	
Surface Treatment	Anti-Glare	-	
EPD driving Waveform	Provided and downloaded by manufacturer		

1-1 General Specification

Note (1): Not including the FPC.

1.4 Mechanical Specification

Item		Min.	Typ.	Max.	Unit	Note
Glass Size	Horizontal(H)	170	170.2	170.4	mm	
	Vertical(V)	111	111.2	111.4	mm	
	Thickness(T)	1.0	1.1	1.2	mm	(1)
Weight		-	TBD	-	g	(2)

Note (1): Not including the Masking Film. (2) Weight for reference only

1.5 FPC Specification

Item	Pin numbers	Pitch (mm)	Connector	Note
Golden Finger	24	0.5	HRS FH34SRJ34S or STARCONN 6700S34 or Compatible	

2. Absolute Maximum Ratings

2.1 Absolute Ratings of Environment

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T_{ST}	-20	+60	ºC	(1),(3),(4)
Storage Humidity	H_{ST}	40	70	%RH	(1),(3),(4)
Operating Ambient Temperature	T_{OP}	0	+35	ºC	(1),(2),(3),(4)
Operating Ambient Humidity	H_{OP}	40	70	%RH	(1),(2),(3),(4)

2-1 Absolute Ratings of Environment

Note (1): (a)70 %RH Max. (Ta ≦ 40 ºC), 40%RH Min. (Ta ≦ 60 ºC) where Ta is ambient temperature.
(b) No condensation and no frost in absolute ratings of Environment.

Note (2): The temperature of panel display surface area should be 0 ºC Min. and 40ºC Max. Refresh time depends on operating temperature.

Note (3): Reddish on the edge of black image is normal at high temperature.

Note (4): EInk Material is Moisture and UV sensitive. The absolute rating operating environments describes the boundary conditions for updating the display while the absolute rating storage environment describe the boundary conditions for a display not updating. While displays are rated to perform according to specification for the warranty period at the absolute specified operating environment, the better the storage condition, the better the E Ink displays will perform. Similar to other moisture and UV sensitive components, we recommend that our displays be stored in temperature and humidity control environments, and whenever possible, under above defined Optimal Storage Condition, away from sunlight, to optimize their performance.

2.2 Reliability Test Item

Item	Test Condition	Remark
Low Temperature Operation	0 ℃ for 240h	(1) (2)
High Temperature/Humidity Operation	40 ℃ / 70 %RH for 240h	(1) (2)
High Temperature Storage	60 ℃ / 40 %RH for 240h	(1)(2)(3)
Low Temperature Storage	-20 ℃ for 240h	(1)(2)(3)
High Temperature/Humidity Storage	50 ℃ / 80 %RH for 240h	(1)(2)(3)
Thermal Cycles (Non-operation)	1 Cycle:-20℃/30min → 60℃/30min, for 100 Cycles	(1)(2)(3)
Package Drop Test	Drop from 97cm. (ISTA) 1 corner, 3 edges, 6 sides. One drop for each.	(1)(2)(3)
Package Random VibrationTest	1.15Grms, 1Hz ~ 200Hz. (ISTA)	(1)(2)(3)

2-2 Reliability Test Item

Note (1): No condensation and no frost during test. End of test, function, mechanical, and optical shall be satisfied.

Note (2): The test result and judgment are based on OTP driving waveform.

Note (3): Stay white pattern for storage and non-operation test.

3. Electrical Characteristics

3.1 Absolute Maximum Ratings of Panel

Parameter	Symbol	Value		Unit	Note
		Min	Max		
Supply Voltage	V_{DD}, V_{DDIO}	-0.3	6.0	V	
Ground	GND	-		-	Connect to Ground

T_a = 25 ± 2 ºC

3.2 Recommended Operation Conditions of Panel

Parameter		Symbol	Value			Unit	Note
			Min	Typ	Max		
VDDIO, VDD operation voltage		V_{DDIO}, VCI	2.3	3.3	3.6	V	
Input Voltage	High	V_{IH}	0.7V_{DDIO}	-	V_{DDIO}	V	V_{DDIO}=V_{DD}
	Low	V_{IL}	0	-	0.3V_{DDIO}	V	
Output Voltage	High	V_{OH}	V_{DDIO}-0.4	-	-	V	V_{DDIO}=V_{DD} I_{OH}=400uA
	Low	V_{OL}	0	-	0.4	V	V_{DDIO}=V_{DD} I_{OL}=-400uA,
Input Current（Mean）		I_{VCI}	-	7	-	mA	(1),(2),(3)
Input Current （Peak）		I_{VCI}	-	212.9	-	mA	(1),(2),(3)
Input Power		-	-	275	-	mA.s	(1),(2),(3)

T_a = 25 ± 2 ºC

Note (1) : Test Pattern of Panel

Note (2) :

$V_{DDIO}=V_{DD}=3.0V$

Image Update Current Profile

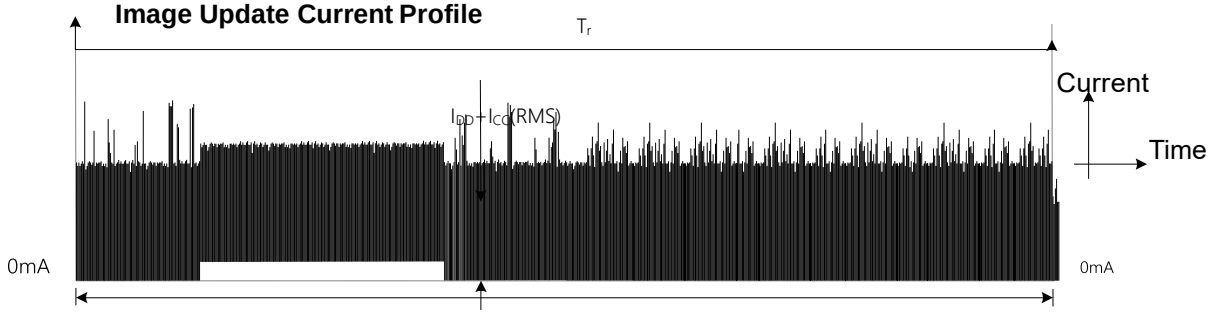
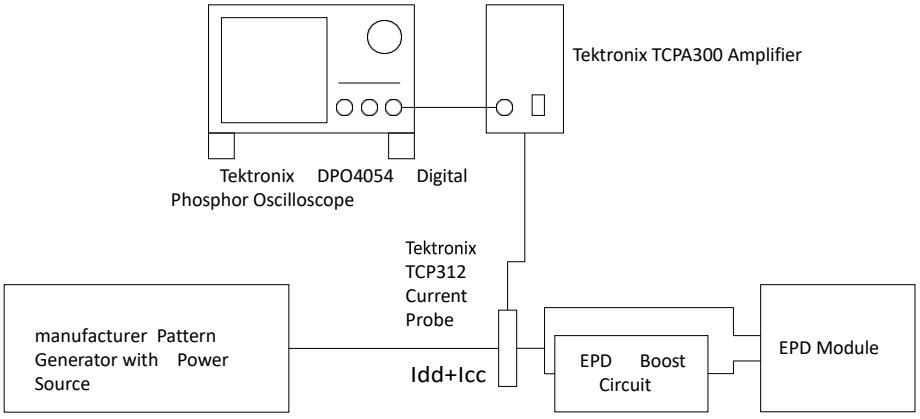


Image Update Time

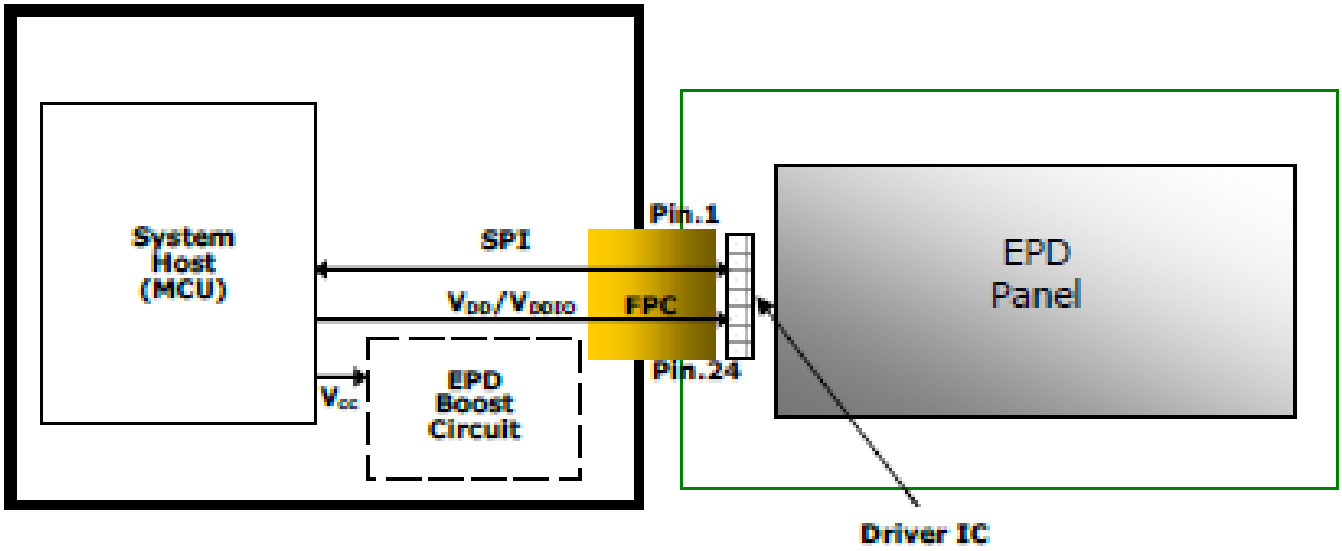
* T_r : Refresh time of the image update.

Note (3): I_{DD}: The current of V_{DD} + V_{DDIO}.
I_{CC} : The current of V_{CC}(EPD Boost Circuit).

Current Measurement



4. Application Circuit Block Diagram



5. Terminal Pin Assignment & Reference Circuit

5.1 Terminal Pin Assignment

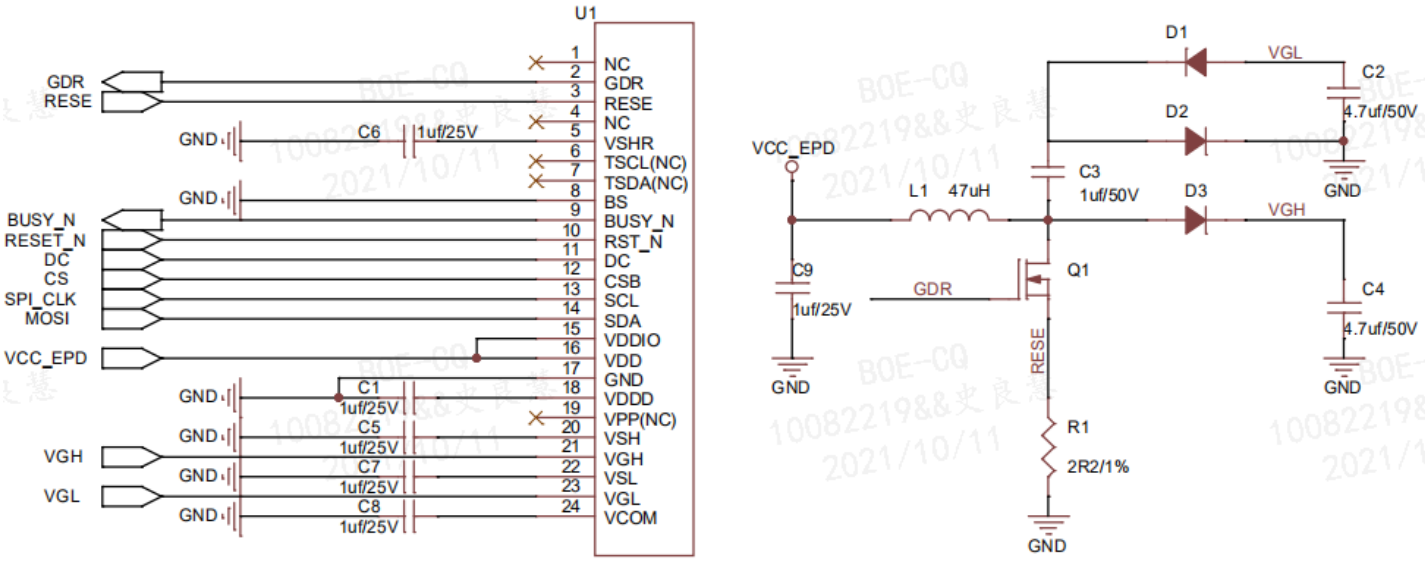
No.	Signal	Type	Connected to	Function
1	NC	-	-	Not connected
2	GDR	O	Power MOSFET Driver control	This pin is the N-Channel MOSFET Gate Drive Control.
3	RESE	I	Booster Control Input	This pin is the Current Sense Input for the Control Loop.
4	NC	-	-	Not connected
5	VSHR	C	Capacitor	This pin is the Positive Gate driving voltage and the Power Supply pin for VDHR. A stabilizing capacitor should be connected between VDHR and GND.
6	TSCL(NC)	-	-	-
7	TSDA(NC)	-	-	-
8	BS	I	VSS	This pin is setting panel interface.
9	BUSY_N	O	Device Busy Signal	This pin is Busy state output pin. When Busy is Low, the operation of the chip should not be interrupted, and Command should not be sent.
10	RES_N	I	System Reset	This pin is reset signal input. Active Low.
11	D/C	I	VDDIO or VSS	This pin is Data/Command control
12	CSB	I	VDDIO or VSS	This pin is the chip select.
13	SCL	I	Data Bus	Serial communication clock input.
14	SDA	I	Data Bus	Serial communication data input/output.
15	VDDIO	P	Power Supply	Power for interface logic pins& I/O. It should be connected with VDDIO.
16	VDD	P	Power Supply	Power Supply for the chip.
17	GND	P	Ground	Ground
18	VDDD	C	Capacitor	Internal regulator output A capacitor should be connected between VDDD and VSS.
19	VPP(NC)	-	-	-

20	VSH	C	Capacitor	This pin is the Positive Source driving voltage. A stabilizing capacitor should be connected between VSH and GND.
21	VGH	C	Capacitor	A stabilizing capacitor should be connected between VGH and GND.
22	VSL	C	Capacitor	This pin is the Negative Source driving voltage and the Power Supply pin for VCOM. A stabilizing capacitor should be connected between VSL and GND.
23	VGL	C	Capacitor	A stabilizing capacitor should be connected between VGL and GND.
24	VCOM	C	Capacitor	This pin is the VCOM driving voltage A stabilizing capacitor should be connected between VCOM and GND.

Note:

Type: I: Input
O: Output
C: Capacitor
P: Power

5.2 Reference Circuit



Part Name	Value/Type	Reference part
C2、C4、C3	4.7uF [Max 50V]	Murata :GRM188R61H475KAALD
C1、C5、C7、C8	1uF [Max 25V]	TDK: C1608X5R1E105K
L1	47uH(DC 0.5A)	Sumida:CDRH2D18/LDNP-470NC
Q1	NMOS	Vishay: Si1304BDL
R1	2.2 Ohm(Current type)	Vishay: CRCW08052R20FKEA
U1	0.5mm ZIF socket	Hirose: FH34S-24S-0.5SH(50)

6. Typical Operating Sequence

6.1 MCU Interface selection

In this module , there are 4-wire SPI and 3-wire SPI that can communicate with MCU.

The MCU interface mode can set by hardware selection on BS1 pins. When it is “Low ”,4-wire SPI is selected. When it is “High”,3-wire SPI(9 bits SPI) is selected.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	D1	D0	CS#	D/C#	RES#
SPI4	SDA	SCL	CS#	D/C#	RES#
SPI3	SDA	SCL	CS#	L	RES#

Table 6-1 MCU interface assignment under different bus interface mode

Note: L is connected to VSS; H is connected to VCI

6.1.1 MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCL, serial data SDA，D/C#，CS#，In SPI mode，D0 acts as SCL，D1 acts as SDA

Function	CS#	D/C#	SCL
Write Command	L	L	↑
Write data	L	H	↑

Table 6-2 Control pins of 4-wire Serial Peripheral interface

Note: ↑ stands for rising edge of signal

SDA is shifted into an 8-bit shift register in the order of D7，D6，…D0. The data byte in the shift register is written to the Graphic Display Data RAM (RAM)/ Data Byte register or command Byte register according to D/C# pin.

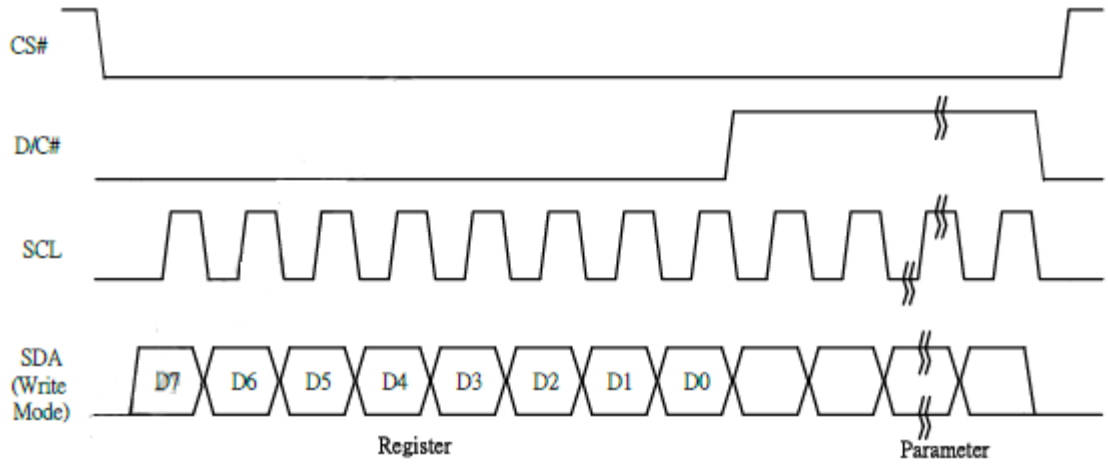


Figure 6-1 Write procedure in 4-wire SPI mode

6.1.2 MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial SCL，serial data SDA and CS#.

In 3-wire SPI mode，D0 acts as SCL ,D1 acts as SDA，The pin D/C# can be connected to an external ground.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit , D/C bit, D7 to D0 bit，The D/C# bit (first bit of the sequential data)will determine the following data byte in shift register is written to the Display Data RAM(D/C# bit =1) or the command register (D/C# bit = 0). Under serial mode , only write operations are allowed.

Function	CS#	D/C#	SCL
Write command	L	Tie to Low	↑
Write data	L	Tie to Low	↑

Table 6-3 Control pins of 3-wire Serial Peripheral interface

Note: ↑ stands for rising edge of signal

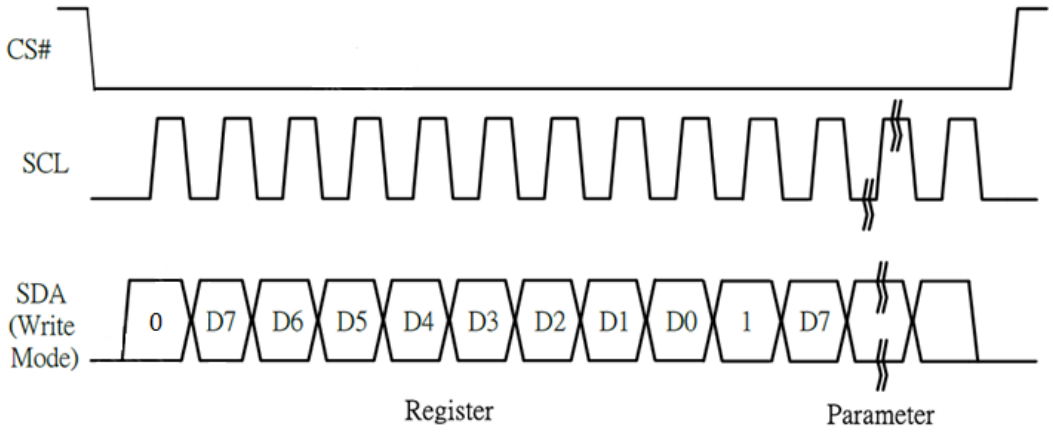
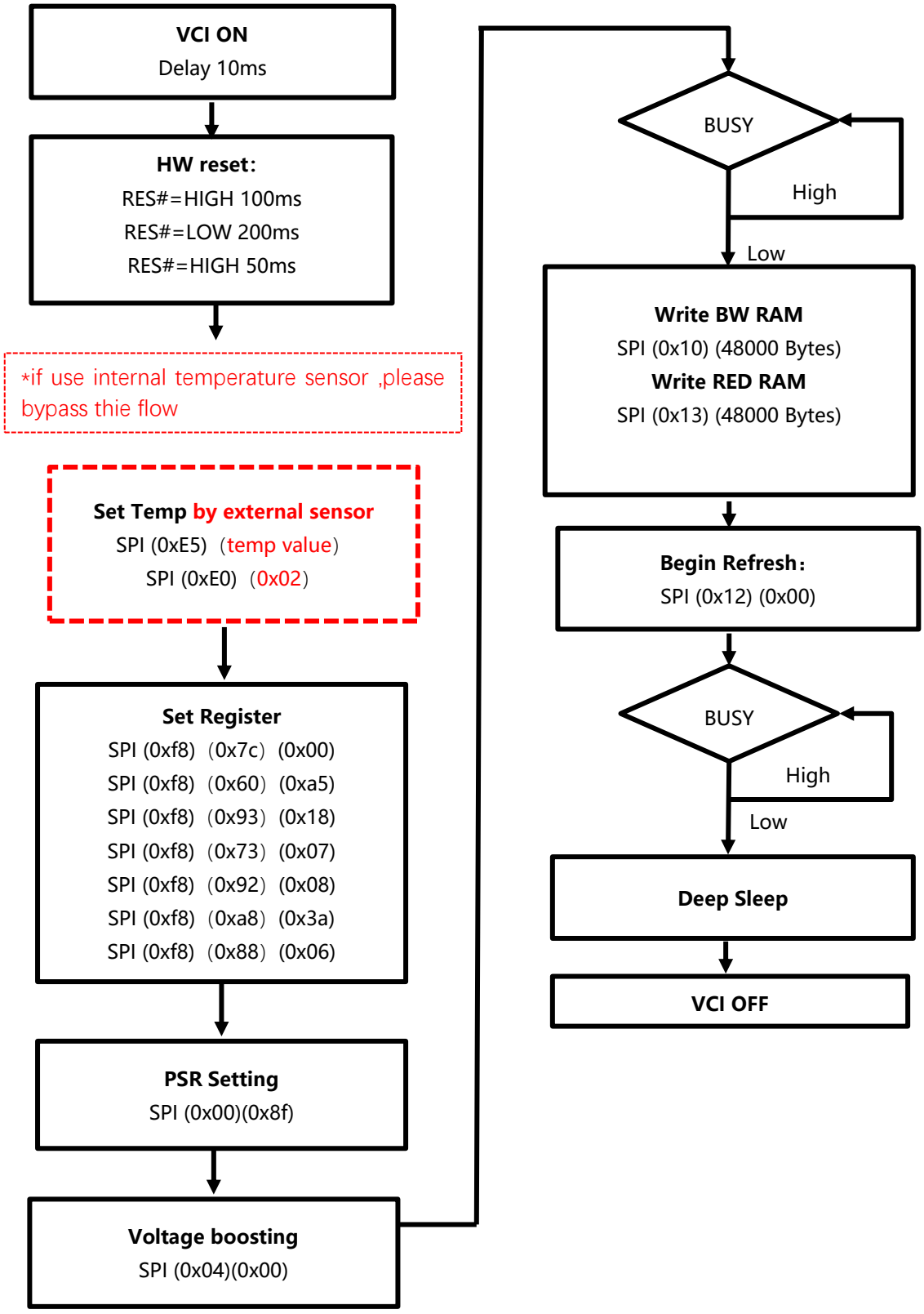


Figure 6-2 Write procedure in 3-wire SPI mode

6.2 Operation Flow



7. Optical Characteristics

7.1 Test Conditions

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	ºC
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V_{DD}	3.0	V

Note (1): Image is updated with above condition.

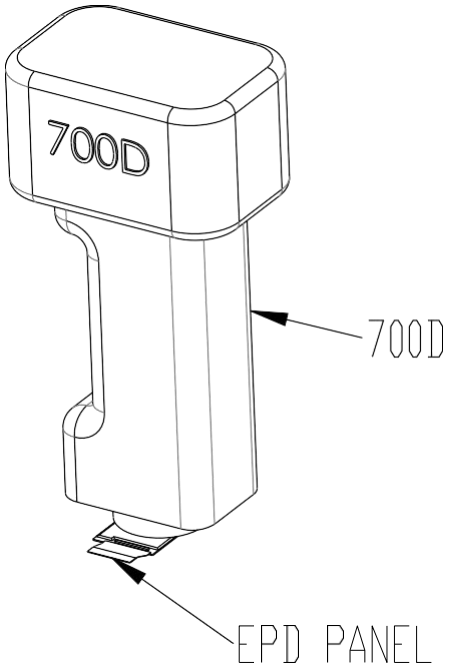
7.2 Optical Specifications

7.2.1 Optical

Item	Color	Symbol	Rating			Unit	Note
			Min.	Typ.	Max.		
Contrast ratio	White/Black	CR	-	20:1	-	-	θx=θy=0 (1),(2),(5),(6)
Refresh time	Black/ White/ Red	Tr	-	24	-	sec	(1),(3),(4),(6)
White state	White	L*	-	65	-	-	θx=θy=0 (1),(2),(6)
	White	a*		0			
	White	b*	-	0.74	-		
Red state	Red	L*	-	25	-		θx=θy=0 (1),(2),(6)
	Red	a*		37			
	Red	b*		22			
Reflectance	White	R%		37			(1),(2),(6)

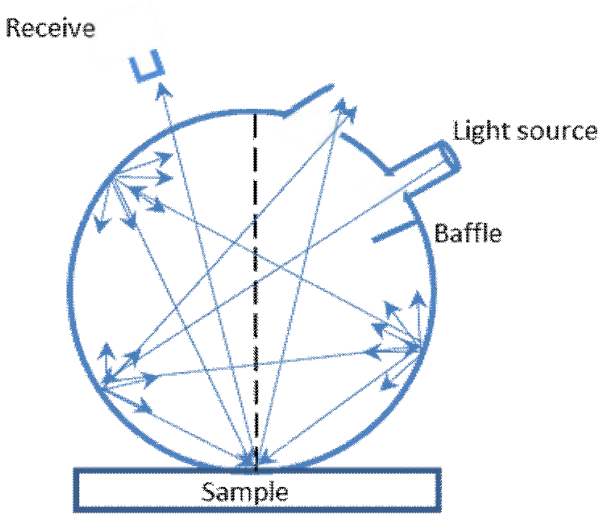
Note (1): Panel is driven by manufacturer waveform without masking film and optical measurement by CM-700D with D65 light source and SCE mode.

Figure 7-1 Optical measurement



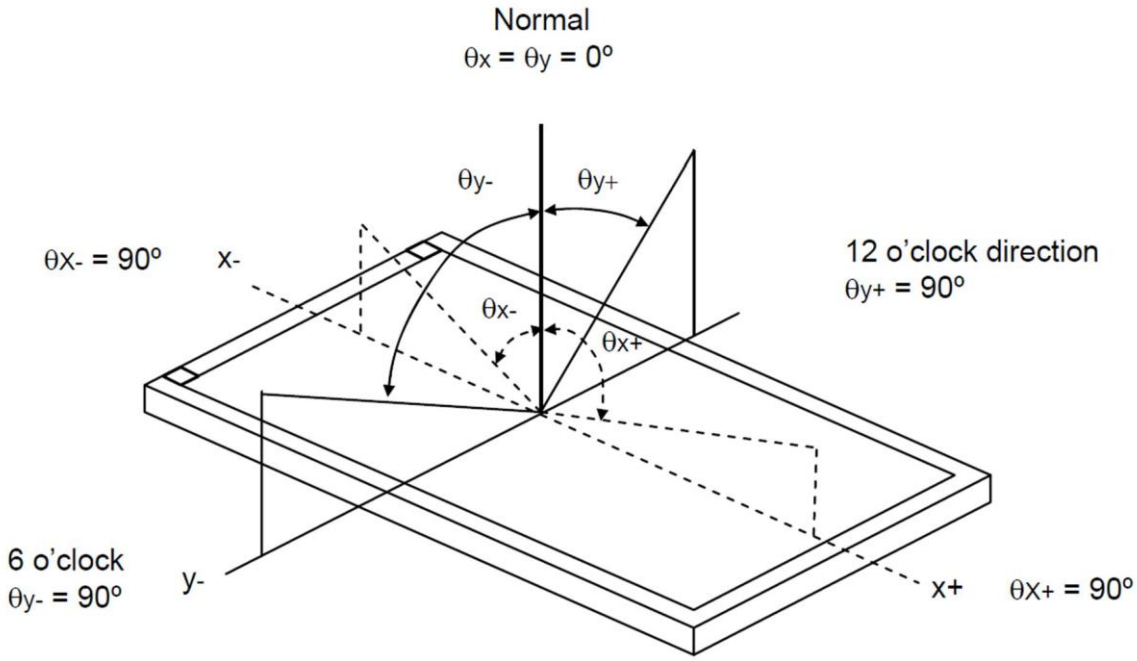
(Face up and remove protection film)

SCE mode



Note (2): Definition of Viewing Angle (x, y)

Figure 7-2Definition of Viewing Angle to Measure Contrast Ratio



Note (3): Refresh time is the time that e-paper particles move not including the power on and off time.

The refresh time is measured at 25 ºC. The refresh time and contrast ratio varies due to different films, display performance requirements, and ambient temperatures.

Note (4): Tr is the refresh time for an image which has no Red. For an image with Red, Red/White, Red/Black, or Red/Black/White, the total update time is (Tr).

Note (5): Contrast ratio (C.R.): The Contrast ratio is calculated by the following expression.
C.R. =(R% White)/(R% Black).

Note (6): Optical data is measured at 60 seconds after refresh with manufacturer's global update procedure.

7.2.2 Ghosting

Below are test method to verify if ghosting is within an acceptable range. The measured data (L*, a*, b*) to calculate color different, $\triangle E_{00}$ (CIEDE 2000).The condition of measurement is to follow " Table 7-1 Optical Measurement Conditions".

Ghosting Measurement

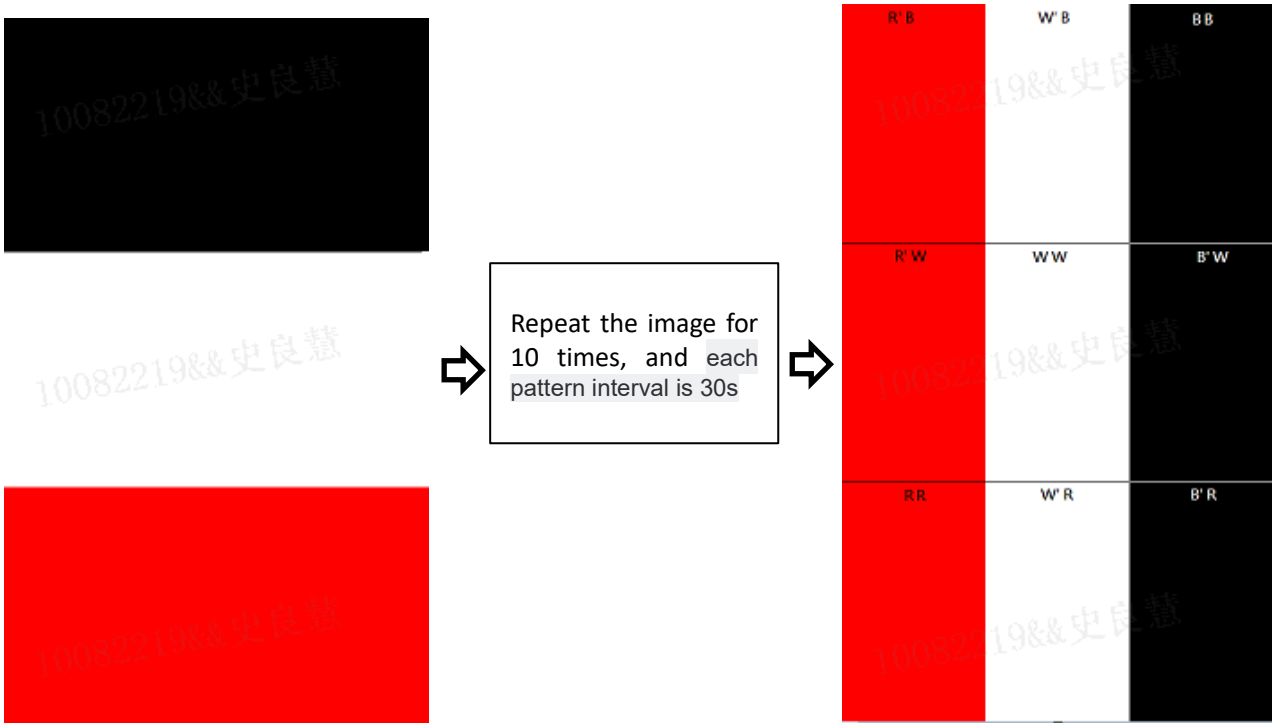
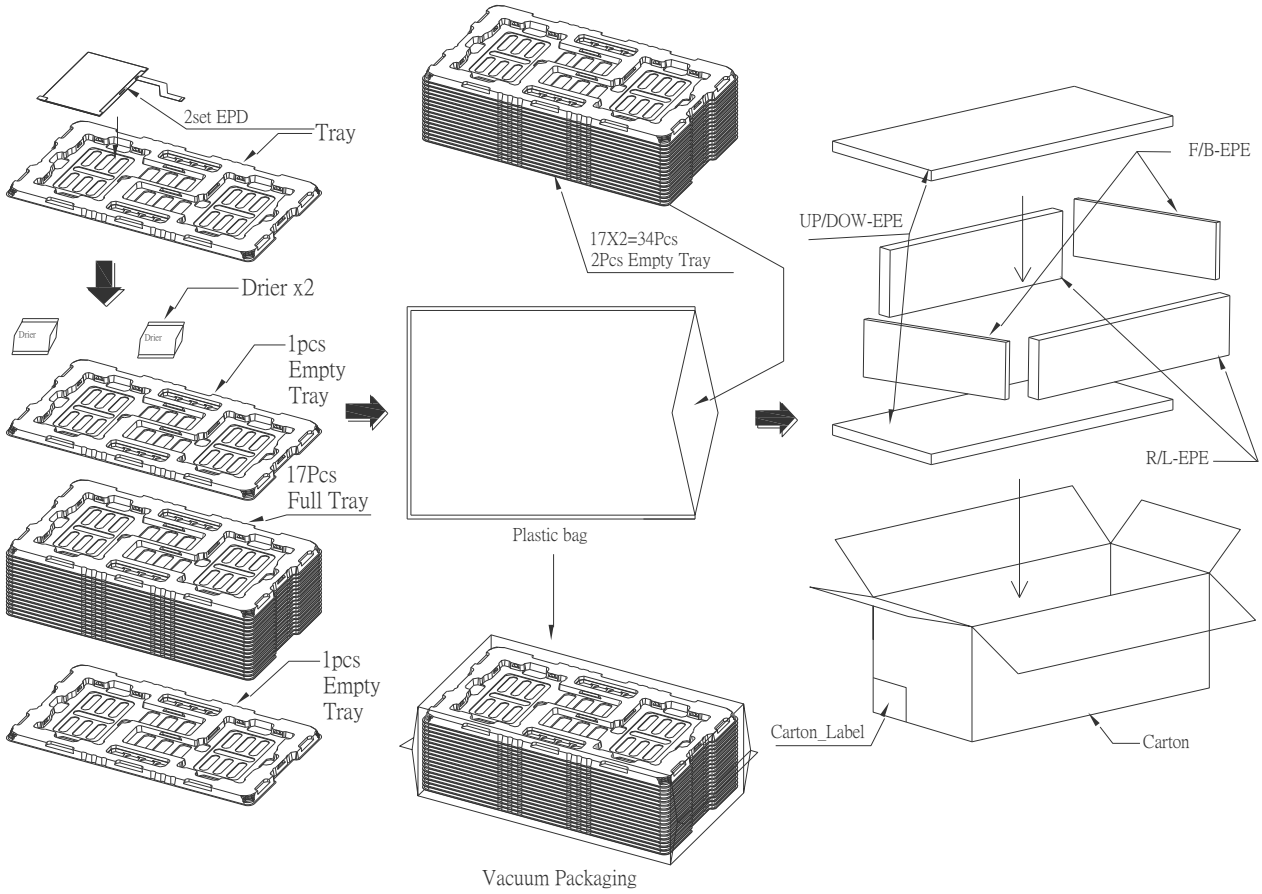


Table 7-3 Measurement of Ghosting

Item	Rating		
	Min.	Typ.	Max.
B'W$\triangle E_{00}$	-	-	2
W'B$\triangle E_{00}$	-	-	2
R'W$\triangle E_{00}$	-	-	4
W'R$\triangle E_{00}$	-	-	2
B'R$\triangle E_{00}$	-	-	2
R'B$\triangle E_{00}$	-	-	4

Note: Panel is driven by manufacturer waveform without masking film and optical measurement by" CM-700D "with D65 light source and SCE mode.

8. Packing



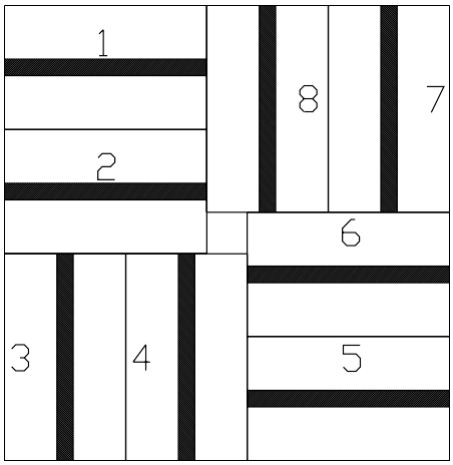


Figure 8.1 Packing

Note: The package method of Figure 8.1 is just for reference, the actual packing number refer to actual production.

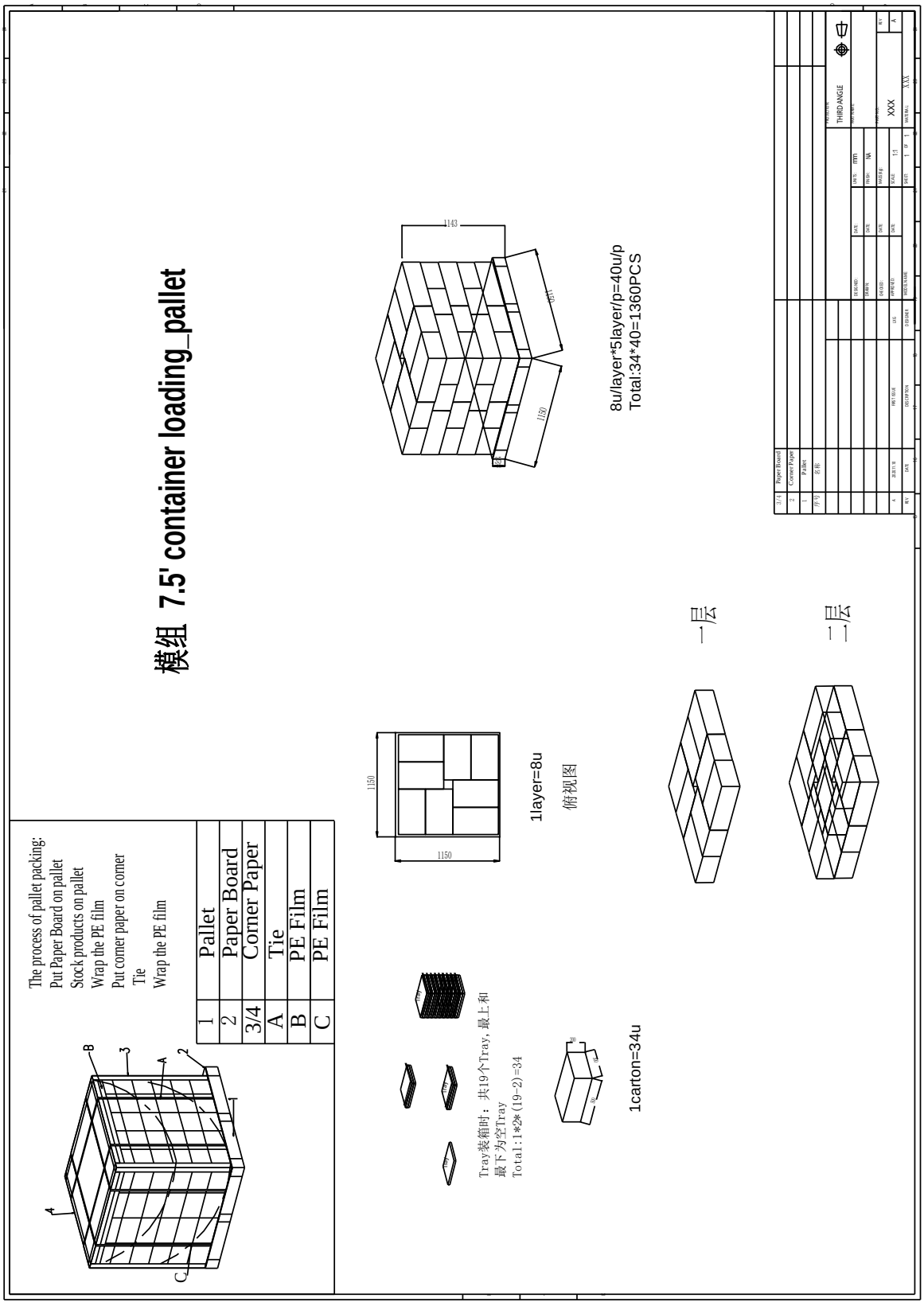


Figure 8.1 Stack

9. EPD Drawing

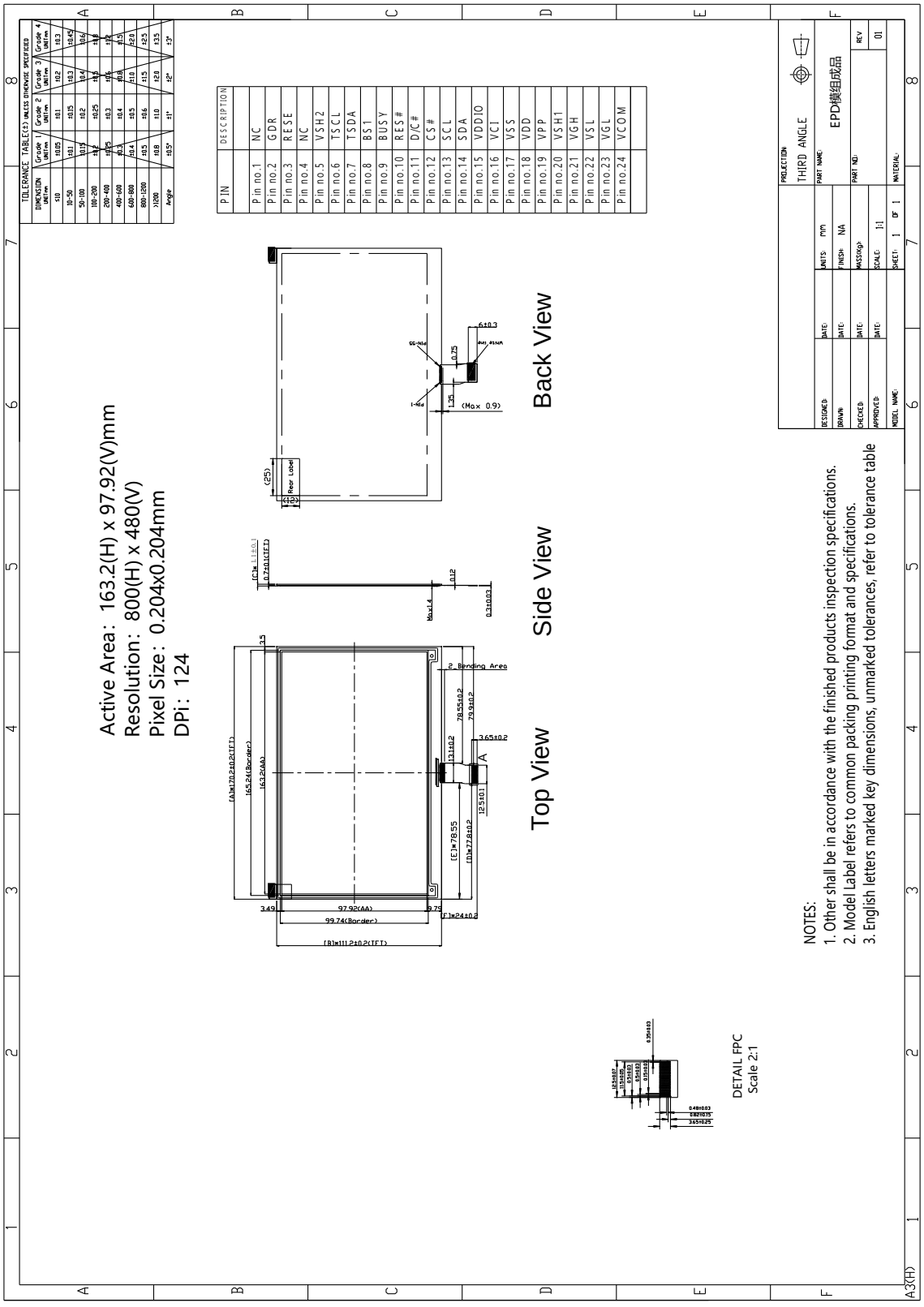


Figure 9.1 EPD Drawing

10. Precaution

(1) The EPD Panel / Module is manufactured from fragile materials such as glass and plastic, and may be broken or cracked if dropped. Please handle with care. Do not apply force such as bending or twisting to the EPD panel.

(2) It is recommended to assemble or install EPD panels in a clean working area. Dust and oil may cause electrical shorts or degrade / scratch / dent the protection sheet film.

(3) Do not apply pressure to the EPD panel in order to prevent damaging it.

(4) Do not connect or disconnect the interface connector while the EPD panel is in operation.

(5) Please support the bezel with your finger while connecting the interface cable such as the FPC.

(6) Do not stack the EPD panels / Modules.

(7) Do not press the FPC on the glass edge or Pull FPC up / down to 90°.

(8) Do not touch the FPC lead connector.

(9) Do not touch IC bonding area. It may scratch TFT lead or damage IC function.

(10) Wear a Wrist Strap (Grounding connect) when handling and during assembly. Semiconductor devices are included in the EPD Panel / Module and they should be handled with care to prevent any electrostatic discharge (ESD). (An Ion Fan may be needed in assembly operation to reduce ESD risk.)

(11) Keep the EPD Panel / Module in the specified environment and original packing boxes when storage in order to avoid scratching and keep original performance.

(12) Do not disassemble or reassemble the EPD panel.

(13) Use a soft dry cloth without chemicals for cleaning. Please don't press hard for cleaning because the surface of the protection sheet film is very soft and without hard coating. This behavior would make dent or scratch on protection sheet.

(14) Please be mindful of moisture to avoid its penetration into the EPD panel, which may cause damage during operation.

(15) It's low temperature operation product. Please be mindful the temperature different to make frost or dew on the surface of EPD panel. Moisture may penetrate into the EPD panel because of frost or dew on surface of EPD panel, and makes EPD panel damage.

(16) High temperature, high humidity, sunlight or fluorescent light may degrade the EPD panel's performance. Please do not expose the unprotected EPD panel to high temperature, high humidity, sunlight, or fluorescent for long periods of time. Please store the EPD panel in controllable environment of warehouse and original package: Without sunlight, without condensation, a temperature range of 5ºC to 35ºC, and humidity from 45%RH to 70%RH.

(17) If the EPD Panel / Module is not refreshed every 24 hours, a phenomena known as "Ghosting" or "Image Sticking" may occur. It is recommended that customer refreshed the ESL / EPD Tag every 24 hours in use case with white image. It is recommended that customer ships or stores the ESL / EPD Tag with a completely white image to avoid this issue.

(18) The label ink used for marking the Panel ID number is erased easily by solvent. Please avoid using solvent to clean the EPD panel.

(19) The EPD is vacuum packed.

(20) Before approved by us and customer, products and product specifications may be subject to change without notice. Confirm that you have received the latest product standards or specifications before final design, purchase or use.

(21) We makes every attempt to ensure that its products are of high quality and reliability. However, contact We sales office before using the product in an application that demands especially high quality and reliability or where its failure or malfunction may directly threaten human life or cause risk of bodily injury, such as aerospace, aeronautics, nuclear power, combustion control, transportation, traffic, safety equipment or medical equipment for life support.

(22) Design your application so that the product is used within the ranges guaranteed by our particularly for maximum rating, operating supply voltage range, heat radiation characteristics, installation conditions and other characteristics. We bears no responsibility for failure or damage when used beyond the guaranteed ranges. Even within the guaranteed ranges, consider normally foreseeable failure rates or failure modes in semiconductor devices and employ systemic measures such as fail safes, so that the equipment incorporating our product does not cause bodily injury, fire or other consequential damage due to operation of the our product.

(23) This product is not designed to be radiation resist

11. Definition of Labels

11.1 Definition of Production Label

TBD

Figure 11.1 Definition of Production Label

11.2 Definition of Pallet Label

TBD

Figure 11.2 Definition of Pallet Label

11.3 Definition of Carton Label

TBD

Figure 11.3 Definition of Carton